Edge-Triggered Flip-Flop

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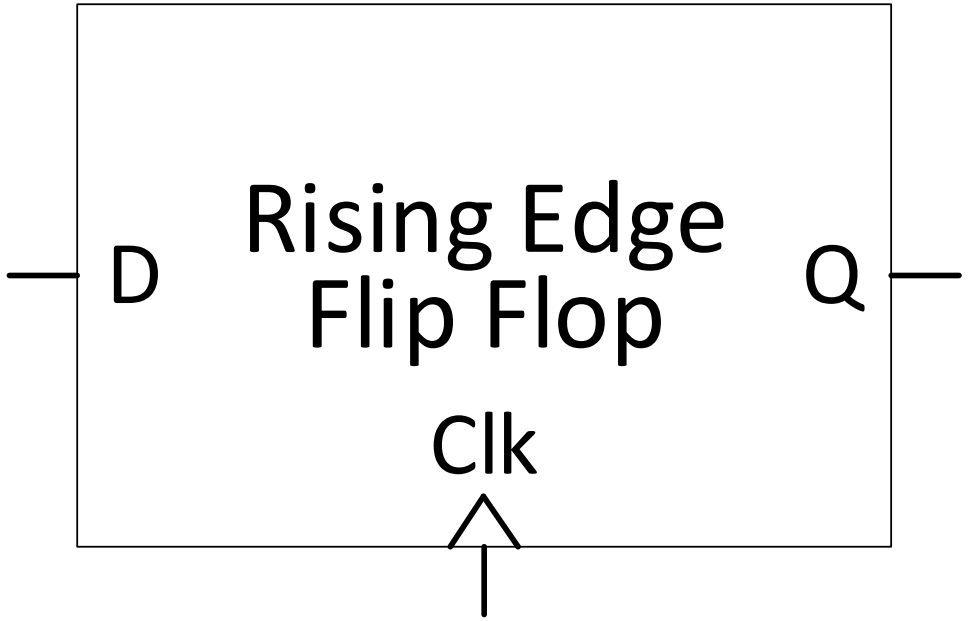
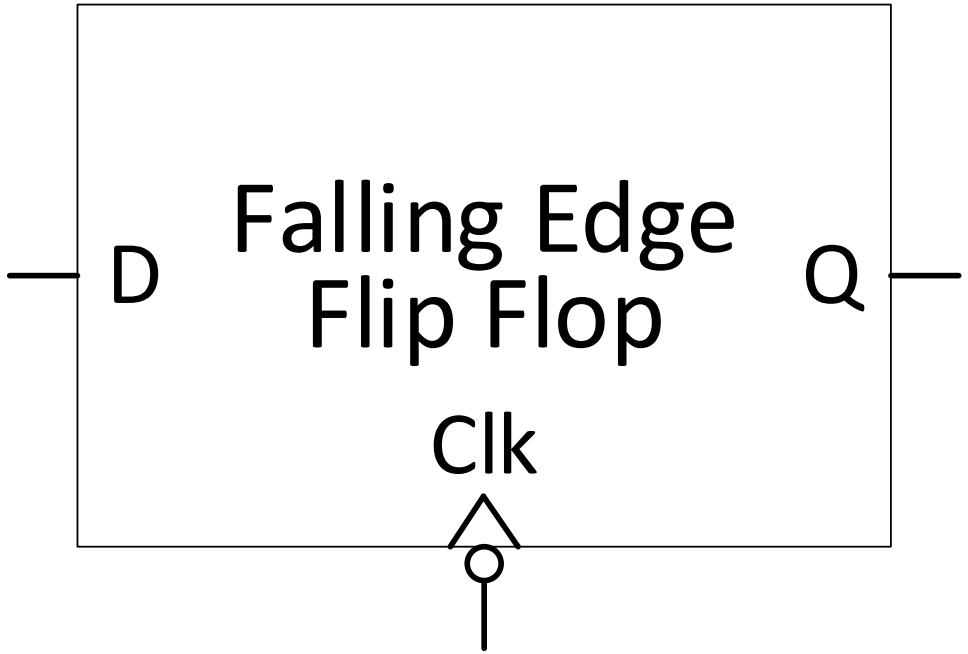
Edge-Triggered Flip-Flop

- An edge-triggered flip-flop is a memory component that stores a single bit value
  - Similar to a flip-flop, but the input is committed to be stored on the transition of a clock signal
    - The operative edge of the clock can be either a rising edge or a falling edge
  - There are still required set-up and hold timing constraints
    - That is, the input data must be stable for some period of time before and after the clock edge

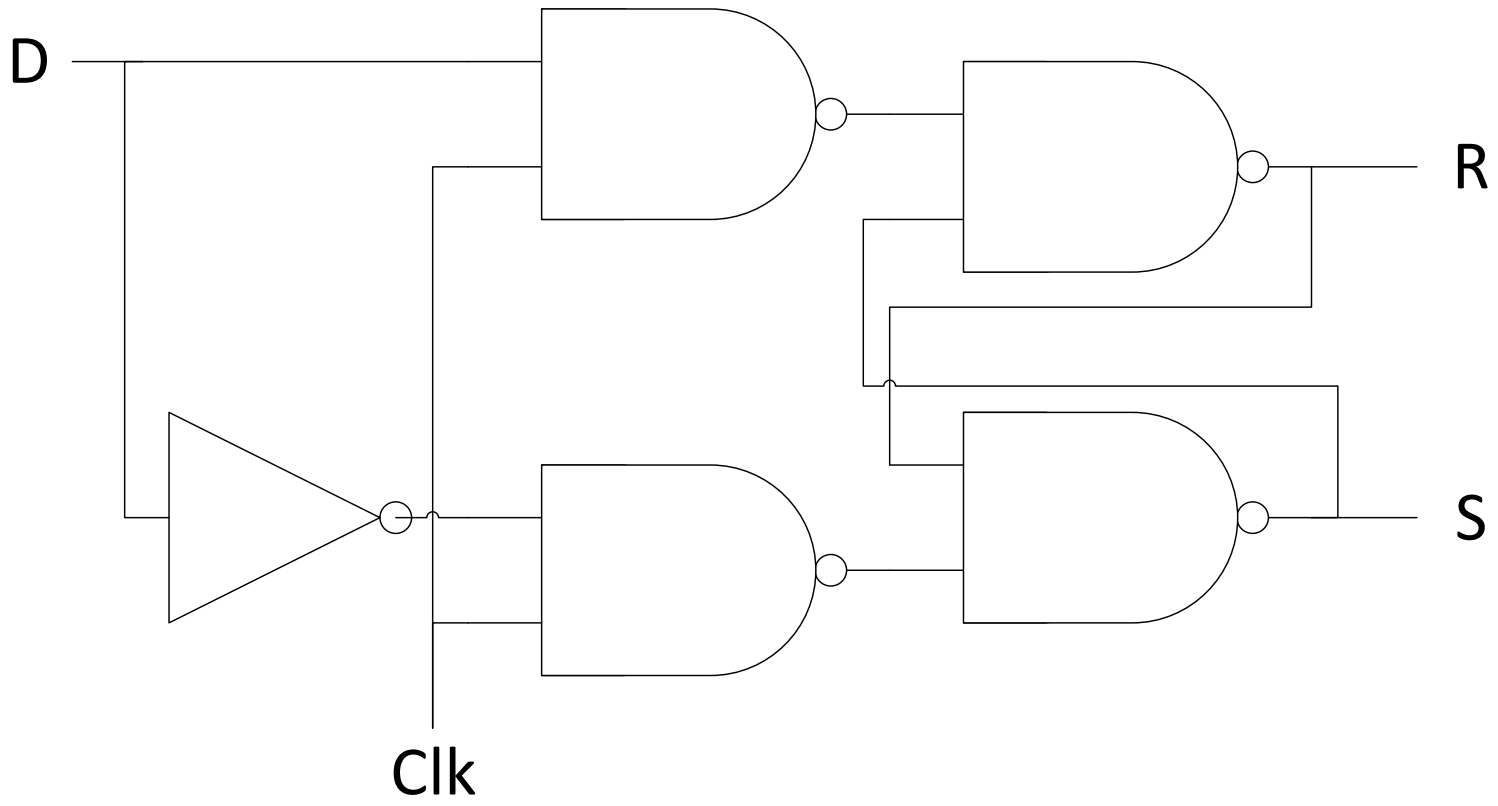
Encapsulation of Rising Edge-Triggered Flip-Flop



Encapsulation of Falling Edge-Triggered Flip-Flop

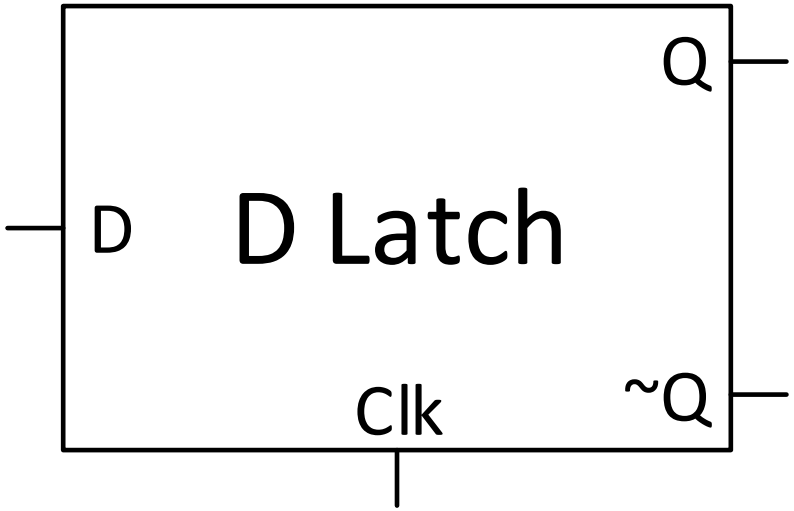


D Latch



D	Clk	R	S
X	0	$\sim S_0 = R_0$	$\sim R_0 = S_0$
D	1	D	~D

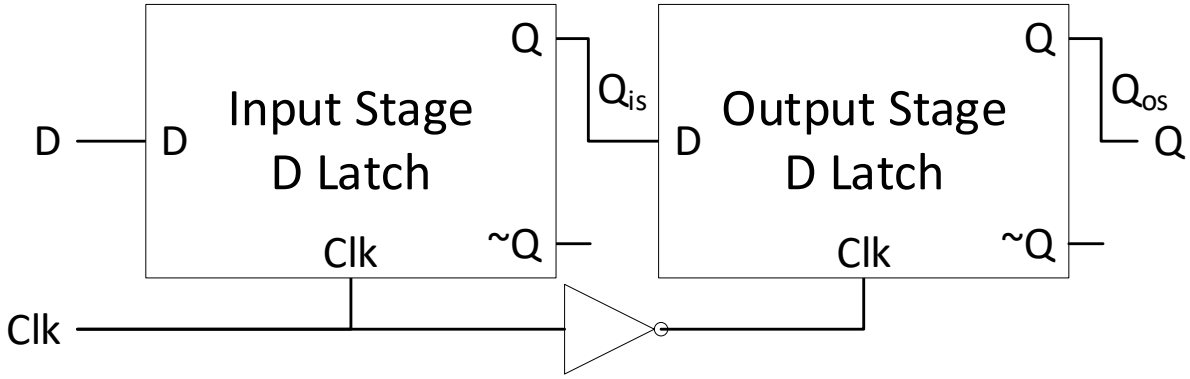
Encapsulation of D Latch



Derivation of an Edge-Triggered Flip-Flop from a D Latch

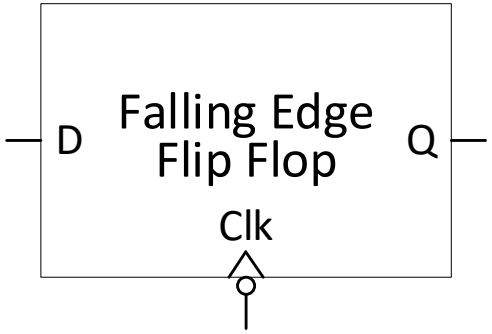
- Use two D latches
  - The two D latches are in opposite states (*i.e.,* when one is passing-through, the other is storing and vice versa)
  - Connect the output of the first latch (the *input stage* latch) to the input of the second latch (the *output stage* latch)
    - We refer to this as a *Master-Slave* configuration
- We need to understand what happens when the clock is stable and also on the clock transitions

Master-Slave Falling-Edge D Flip-Flop



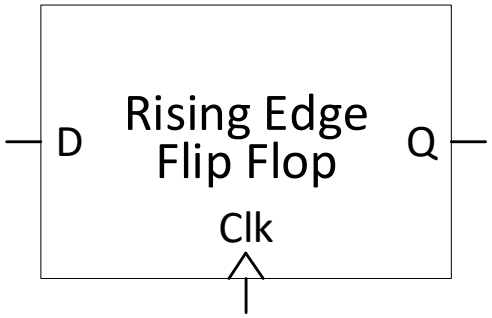
D	Clk	Input Stage	Q_{is}	Output Stage	Q == Q_{os}
X	0	Store	Q_{is_0}	Pass-through	Q_{is}
D	↑		D		Q_{is}
D	1	Pass-through	D	Store	Q_{os_0} == Q_{is}
X	↓		Q_{is_0}		D

Master-Slave Falling-Edge D Flip-Flop



D	Clk	Q
X	0	Q_0
X	↑	Q_0
X	1	Q_0
D	↓	D

Master-Slave Rising-Edge D Flip-Flop



D	Clk	Q
X	0	Q_0
D	↑	D
X	1	Q_0
X	↓	Q_0